We claim:

1. A data link layer processor comprising:

one or more media access controllers (MACs);

a traffic policer, operatively coupled to the one or more MACs, for discarding frames received from the MACs that exceed a bandwidth parameter; and

a MAC buffer, operatively the traffic policer, for buffering allowed frames received from the traffic policer.

2. A switching device comprising:

one or more physical layer interfaces for receiving a plurality of frames from a communication network;

a plurality of data link layer processors, wherein each data link layer processor comprises:

one or more MACs, wherein each MAC is operatively coupled to a physical layer interface; and

a traffic policer, operatively coupled to the one or more MACs, for discarding one or more of the plurality of frames received from the MACs that exceed one or more bandwidth parameters; and

a network processor, operatively coupled to the plurality of data link layer processors, for routing the frames received from the plurality of data link layer processors.

3. The switching device of claim 2, wherein the traffic policer discards the one or more of the plurality of frames in accordance with a Three Color Marker (TCM) algorithm.

4. The switching device of claim 3, wherein the TCM algorithm is selected from the group consisting of: single rate TCM, two rate TCM, and a combination thereof.

5. The switching device of claim 2, wherein the traffic policer comprises:

an ingress meter module for determining a flow rate associated with the plurality

of frames received by the associated data link layer processor; and

a discard control logic for selectively discarding the one or more frames based upon the flow rate and the one or more bandwidth parameters.

6. The switching device of claim 5, wherein the traffic policer further comprises a marker module for marking the plurality of frames in accordance with a TCM algorithm.

7. The switching device of claim 6, wherein the one or more bandwidth parameters comprise a committed information rate (CIR) and an excess burst size (EBS).

8. The switching device of claim 2, wherein the traffic policer comprises a flow search engine for classifying the plurality of frames based upon one or more properties associated with the frames.

9. The switching device of claim 8, wherein the flow search engine comprises a content addressable memory (CAM).

10. The switching device of claim 8, wherein one or more properties comprise a source port, a VLAN tag state, a VLAN identifier, and a VLAN tag control information (TCI) field.

11. The switching device of claim 8, wherein the CAM associated with each of the plurality of data link layer processors consists of QoS rules pertaining to the associated plurality of physical layer interfaces.

12. The switching device of claim 2, wherein data link layer processors are media access controller (MAC) processors.

13. The switching device of claim 12, wherein each of the MAC processors further comprises a MAC buffer for buffering frames not discard by the traffic policer.

14. The switching device of claim 2, wherein the switching device is selected from the group consisting of: a router, a multi-layer switching device, and a switch blade.